REMARKS

In response to the Office Action mailed May 20, 2005, Applicant respectfully requests reconsideration.

Claims 1-11 have been previously examined and are pending for examination, of which claims 1, 6 and 9 are independent. No amendments have been made in this Request.

1. Claims 1-5 Patentably Distinguish Over Callahan II

Claim 1 stands rejected under §102(e) as being anticipated by U.S. Patent No. 6,321,379 (Callahan II). Applicant respectfully traverses this rejection.

Callahan II discloses that a target register allocation (TRA) system receives blocks of code including branches, and determines where to locate target register definitions for branches within the blocks. (Abstract, lines 1-3; col. 3, lines 51-65). A target definition defines a target address for a branch, which is loaded into a target register. (Col. 2, lines 36-38) Notably, the target register definitions are not included in the blocks of code received and read by the TRA, but rather, are inserted by the TRA. That is, if the TRA system determines that a block includes a branch, then it executes a routine that creates a live range for the block and branch. (Figs. 7, step 708; col. 9, lines 19-20) This routine sets the *initial* location of a target register definition for the branch within the block. (Col. 11, lines 33-35; emphasis added).

In contrast, claim 1 recites:

> A method of compiling a computer program from a sequence of **computer instructions including a plurality of first, set branch, instructions which each identify a target address for a branch** and a plurality of associated second, effect branch instructions which each implement a branch to a target address, the method comprising:
>
> **reading said computer instructions** in blocks;
>
> defining a set of target registers associated with each block for holding target addresses for the set branch instructions in that block;
>
> defining as a live range of blocks a set of blocks for which a target address of a particular set branch instruction is in a live state; and
>
> using said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses.

Claim 1 patentably distinguishes over Callahan II because Callahan II does not teach or suggest a method of compiling a computer program from a sequence of computer instructions

including a plurality of first, set branch, instructions which each identify a target address for a branch and a plurality of associated second, effect branch instructions which each implement a branch to a target address, the method comprising, inter alia, reading said computer instructions in blocks, as recited in claim 1. Rather, as noted above, Callahan II discloses that target definitions defining target addresses for branches are inserted into blocks of code only *after* these blocks of code are read by the TRA.

In view of the foregoing, claim 1 patentably distinguishes over Callahan II. Accordingly, Applicant respectfully requests that the rejection of claim 1 under §102(e) be withdrawn. Claims 2-5 depend from claim 1 and are patentable for at least the same reasons. Accordingly, Applicant respectfully requests that the rejections of these claims be withdrawn.

2. **Claims 6-8 Patentably Distinguish Over Callahan II**

Claim 6 stands rejected under §102(e) as being anticipated by Callahan II. Applicant respectfully traverses this rejection.

Claim 6 recites:

> A method of operating a computer system to compile a computer program from a sequence of **computer instructions including a plurality of first, set branch instructions which each identify a target address for a branch** and a plurality of second, effect branch instructions which each implement a branch to the target address specified in the associated set branch instruction, the method comprising:
>
> executing a dominator tree constructor function in the computer system to **read said computer instructions in blocks** and to define a set of target registers associated with each block for holding target addresses for the set branch instructions in that block;
>
> executing a lifetime tracking algorithm to define as a live range of blocks a set of blocks for which a target address of a particular set branch instruction is in a live state, said lifetime tracking algorithm being operable to use said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses.

As should be clear from the discussion of Callahan II set forth above in Section 1, Callahan II does not teach or suggest a method of operating a computer system to compile a computer program from a sequence of computer instructions including a plurality of first, set branch instructions which each identify a target address for a branch and a plurality of second,

effect branch instructions which each implement a branch to the target address specified in the associated set branch instruction, the method comprising, *inter alia*, executing a dominator tree constructor function in the computer system to read said computer instructions in blocks, as required by claim 6. Rather, as noted above, Callahan II discloses that target definitions defining target addresses for branches are inserted into blocks of code only after these blocks of code are read by the TRA

In view of the foregoing, claim 6 patentably distinguishes over Callahan II. Accordingly, Applicant respectfully requests that the rejection of claim 6 under §102(e) be withdrawn. Claims 7 and 8 depend from claim 6 and are patentable for at least the same reasons. Accordingly, Applicant respectfully requests that the rejections of these claims be withdrawn.

3. Claims 9-11 Patentably Distinguish Over Callahan II

Claim 9 stands rejected under §102(e) as being anticipated by Callahan II. Applicant respectfully traverses this rejection.

Claim 9 recites:

> A compiler for compiling a computer program from a sequence of **computer instructions including a plurality of first, set branch instructions which each identify a target address for a branch** and a plurality of associated second, effect branch instructions which implement a branch to the target address specified in the associated set branch instruction, the compiler comprising:
>
> a dominator tree constructor for **reading said computer instructions in blocks** and for allocating each set branch instruction to an initial node in a dominator tree, said initial node being located in the block which contains the corresponding effect branch instruction;
>
> circuitry for defining a set of target registers associated with each block for holding target addresses for the set branch instructions in that block;
>
> circuitry for executing a lifetime tracking algorithm which defines as a live range of blocks a set of blocks for which a target address of a particular set branch instruction is in a live state, and which is arranged to use said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses.

As should be clear from the discussion of Callahan II set forth above in Section 1, Callahan II does not teach or suggest a compiler for compiling a computer program from a sequence of computer instructions including a plurality of first, set branch instructions which

each identify a target address for a branch and a plurality of associated second effect branch instructions which implement a branch to the target address specified in the associated set branch instruction, the compiler comprising, *inter alia,* a dominator tree constructor for reading said computer instructions in blocks, as required by claim 9.

In view of the foregoing, claim 9 patentably distinguishes over Callahan II. Accordingly, Applicant respectfully requests that the rejection of claim 9 under §102(e) be withdrawn. Claims 10 and 11 depend from claim 9 and are patentable for at least the same reasons. Accordingly, Applicant respectfully requests that the rejections of these claims be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 19, 2005.

Janine Michalski

Attorney Docket No.: S1022.80767US00
X09/20/05X

Respectfully submitted,

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